Marco Spaziani Brunella

Summary

Marco is a hardware engineer specializing in processor architecture and RTL design with eight years of experience across RISC-V cores, AI accelerators, and packet processing systems. Currently at Siliscale Consulting, he owns the decode, scheduling, and execution logic for a massively-parallel RISC-V out-of-order core and has designed fifteen RISC-V ISA extensions covering cryptography, bit manipulation, and conditional operations.

His career includes leading roles at Luminous Computing, where he converted an RV32G core to RV64ICMFD and architected a VLIW vector co-processor, and as CTO at Axbryd, where he managed teams developing 100+ Gbps FPGA-based packet processing accelerators that won the USENIX OSDI 2020 Best Paper Award. At CNIT, he designed reconfigurable VLIW processors supporting multiple ISAs through hardware intermediate representations.

He has extended LLVM backends for custom architectures, developed MLIR dialects for in-memory AI accelerators, and created INT4 quantization for computer vision models. Alongside his engineering work, he runs a technical education business teaching digital design and system administration through Udemy courses and professional mentoring.

Education

University of California, Berkeley — Berkeley, CA
SkyDeck Acceleration Program, Semiconductor Track — April 2022 - September 2023
Relevant Coursework: Patent Law, Hiring and Decision Making, Raising Venture Capital, Public Speaking

University of Rome, Tor vergata — Rome, Italy
Ph.D. in Electrical Engineering, with a minor in Semiconductor Physics. — November 2019 – November 2022

University of Rome, Tor vergata — Rome, Italy
M.Sc. in Electrical Engineering, with a minor in Semiconductor Physics. — October 2017 – October 2019

University of Rome, Tor vergata — Rome, Italy
B.Sc. in Electrical Engineering. — October 2013 – July 2017

Experience

Siliscale Consulting — Remote
Director, Hardware/Software Co-Design — May 2023 – Present

RTL Design

- Owner of the decode, scheduling and execution logic of a massively-parallel RISC-V Out-of-Order core
- Led the integration and verification of a custom, third-party Floating-Point Unit.
- Responsible for the design and initial sign-off of the RTL for the following RISC-V extensions: P, Zicond, Zba, Zbb, Zbc, Zbs, Zbkb, Zbkc, Zbkx, Zknd, Zkne, Zknh, Zksed, Zksh, Zkr, Zkt, Zkn, Zks, Zk

RTL Verification

- Designed an open-source Instruction-Set Simulator (ISS) for hardware verification, fully supporting RISC-V RV64G.
- Designed an open-source Instruction-Set Simulator (ISS) for hardware verification, fully supporting the eBPF instruction set.
- Designed an UVM-based SystemVerilog transactional test-bench for full-chip software simulation and the relevant simulation manager software infrastructure.

Compilers

- Extended Synopsys ARC LLVM Backend to support an in-memory AI Accelerator and it's new ISA extensions
- Developed a new MLIR Dialect for an in-memory AI Accelerator, specifically targeted at Computer Vision workloads
- Developed an INT4 quantizer for an in-memory AI Accelerator, specifically targetting YOLO computer vision models

Luminous Computing Austin, TX (Remote)
Staff RTL Engineer - AI Accelerators November 2021 – April 2023

- Responsible for the conversion of an RV32G open-source core to an RV64ICMFD core while maintaining the Performance-Power-Area figures (PPA).
- Led the Floating-Point Unit design, integration and verification effort.
- Architected and led the RTL design and verification effort of a Very-Long Instruction Word (VLIW) Vector co-processor based on a proprietary ISA for AI applications.
- Led the FPGA-in-the-loop verification methodology, designing the PCI-Express wrapper that was then used throughout the company.

Axbryd Berkeley, CA (Remote)
Chief Technical Officer - Packet Processing Accelerators November 2019 – October 2021

- Led the development of an FPGA-based 100+ Gbps edge packet processing accelerator
- Managed a group of five full-time employees and two contractors, ranging from verification to compiler design
- Responsible for the architecture of the entire accelerator, along with it's design and verification.
- Led the third-party IP integration effort of Ethernet MACs, PCI-e Root Complex, DDR4 and HBM endpoints.
- Awarded USENIX OSDI 2020 Jay Lepreu Best Paper Award

CNIT Rome, Italy
Senior RTL Engineer - Packet Processing Accelerators September 2016 – October 2019

- Led the design and implementation of a reconfigurable Very-Long Instruction Word (VLIW) processor, from architecture specification to RTL microarchitecture implementation.
- The core supported MIPS, RISC-V and eBPF ISA, using an hardware intermediate level representation to abstract the particular implemented ISA.
- Led the Hardware-Software co-design effort, managing a group of 3 people of compiler experts in developing an LLVM backend for the VLIW target